REMARKS

Claims 1-37 are pending in the above-referenced application. Claims 24-37 have been withdrawn from consideration. Claims 1-10, 14-16, 18, and 20-22 are rejected. Claims 11-13, 17, 19, and 23 are objected to. The Office Action is non-final. More specifically and in accord with the item numbers therein, the Office Action has:

In Item 1, acknowledged Applicant's election with traverse, but has found it non-persuasive and thus made the restriction requirement final;

In Item 2, rejected claims 1-10, 14-16, 18, and 21-22 under 35 U.S.C. 102(e) as being anticipated by Choi (U.S. Patent No. 6,538,367); and

In Item 3, indicated that claims 11-13, 17, 19 and 23 are allowable, if rewritten in dependent form including all of the limitations of the base claim and any intervening claims.

Applicant has cancelled claims 1-37 without prejudice or surrender of subject matter and added claims 38 through 75. Reconsideration is requested in light of added claims and remarks. The new independent claims are 38, 39, 58, and 64, claim 38 corresponding to allowable subject matter rewritten in independent form. Claim 39 is an amended version of originally-submitted claim 1 and claim 64 is an amended version of originally-submitted claim 20. Claim 58 is new.

With respect to Item 2 and regarding claims 38, 39, and 64, Applicant submits that the Choi '367 reference fails to teach each and every limitation of Applicant's invention as recited in those claims, because the reference fails to teach the limitation "a gate electrode disposed over the insulator and having one or a plurality of apertures, wherein each aperture exposes a single nano-structure and is concentrically self-aligned with the end of the nano-structure, the gate electrode being operative to control the emission of electrons through the apertures from the exposed nano-structures," which is present in all three claims. Applicant's invention achieves this resulting structure because of the way it is fabricated. In contrast, the reference teaches the use of a particle masking technique to achieve a gate aperture structure. However, the particle masking techniques taught in the reference cannot achieve the limitation set forth and therefore the reference does not teach such a structure. First, the technique in the reference purposefully

includes a multiplicity of nanoconductors in each aperture. Choi, Col. 7, line 64 to Col. 8, line 3. In contrast, Applicant's invention, in claims 38, 39, and 64, recites that each aperture exposes a single nano-structure and is concentrically self-aligned with the end of the nano-structure. Second, the technique in the reference does not contemplate the alignment of an aperture about the end of a nano-structure. This is clear from FIG. 11 of the reference and the description of the particle mask technique. Clearly, the range in the size of the particles (1-5 μm) is such that multiple nano-structures will become exposed by the aperture and thus there is no concept of aligning the aperture with those multiple structures. Choi, Col. 8, lines 46-53. Therefore, the Choi reference fails to teach each and every limitation of Applicant's invention as recited in claims 38, 39, and 64.

With respect to claim 58, Applicant further submits that the Choi reference fails to teach the limitation "one or a plurality of gating means, disposed over the insulator, for controlling the flow of electrons emitted by the nano-structure emitting means, each of said gating means arranged symmetrically relative to one of the nano-structure emitting means." In the reference, there is no possibility that the structures achievable therein could have each gating means arranged symmetrically with respect to one of the nano-structures, as the reference only contemplates a plurality of nano-structures in each aperture. Choi, Col. 7, line 64 to Col. 8, line 3. Therefore, the reference fails to teach each and every limitation of claim 58.

With respect to claims 40-57, Applicant submits that these claims are allowable at least because claim 39, from which they depend, directly or indirectly, is allowable. Additionally, Applicant submits that the Choi reference fails to teach the limitation "wherein the nano-structures protrude above the surface of the emitting layer for not more than half of one micrometer," in claim 44 or the limitation "wherein the apertures in the insulator expose the entire protrusion portion of the nano-structures in the emitting layer," in claim 45, as nothing in Choi teaches or describes any such protrusion. Additionally, Choi fails to teach or describe the limitation "wherein the nano-structures have a coating for enhanced field emission performance," recited in claim 48. Additionally, Choi fails to teach the limitation "wherein the nano-structures comprise a nonconductive core and a conductive shell," as recited in claim 51 or the limitation "wherein the nonconductive core is made from one of wide band gap

semiconductors, including diamond, BN, AlN, AlGaN, GaN, GaAs, SiC, ZnO," recited in claim 52. In fact, the Examiner has indicated that the limitations of claim 48 would make the claims allowable if rewritten in independent form. This Applicant has done in claim 38.

Additionally, the Choi reference fails to teach the limitation "wherein the embedding material is comprised of at least two layers," recited in claim 53, or the limitation "wherein the first layer of the embedding material is conductive," recited in claim 54, as Choi fails to describe any features of any embedding material. Additionally, Choi fails to teach the limitation "wherein the insulator and the embedding material are composed of the same dielectric material," in claim 55 or the limitation "wherein said insulator functions also as the embedding material," in claim 56, again because Choi fails to describe any features of any embedding material. Additionally, Applicant submits that claim 57 is allowable because the Choi reference fails to teach the limitation "wherein the gate electrode is configured as a plurality of electrically isolated electrodes, each intersecting with said cathode electrodes," because Choi does not describe the arrangement of intersecting electrodes. In fact, the Examiner has indicated that claims 55 and 57 would be allowable if rewritten in independent form.

With respect to claims 59-63, Applicant submits that these claims are allowable at least because claim 58, from which they depend, is allowable.

With respect to claims 65-68, Applicant submits that these claims are allowable at least because claim 64, from which they depend, is allowable. Additionally, Applicant submits that the Choi reference fails to teach the limitation "wherein the cathode electrode is configured as a plurality of strip-like cathode electrodes...wherein the gate electrode is configured as a plurality of strip-like gate electrodes extending in such a manner as to intersect said plurality of cathode electrodes," recited in claim 68, because Choi describes no such arrangement of intersecting cathodes and gates. In fact, the Examiner has indicated that the limitation of claim 68, would be allowable if rewritten in independent form.

With respect to claim 38, as mentioned above, Applicant has rewritten originally submitted claim 11 in independent form. Applicant therefore believes these claims are allowable.

Thus, in light of the above, Applicants respectfully request reconsideration and allowance of the pending claims and the new claims in the above-mentioned application.

Respectfully submitted,

Dated: December 1, 2005

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CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that this correspondence is being forwarded via facsimile to Examiner Jesse Fenty in Group No. 2815 at facsimile number 571.273.8300 located at Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA, 22313-1450, on

Date: December 1, 2005

Yolette Yturralde-Owen

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Zhidan TOLT	Docket No.:	nanogate120303
Serial No.:	10/707,342	Group Art Unit:	2815
Filed:	December 5, 2003	Examiner:	Fenty, Jesse
For:	LOW VOLTAGE ELECTRON SOURCE WITH SELF ALIGNED GATE APERTURES, FABRICATION METHOD THEREOF, AND LUMINOUS DISPLAY USING THE ELECTRON SOURCE		

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REQUEST FOR RECONSIDERATION WITH AMENDMENT
UNDER 37 C.F.R. § 1.111 - SUPPLEMENTAL REPLY
(Marked-Up Version)

Sir:

In response to the Notice mailed on November 1, 2005, please consider Applicant's Supplemental Reply. Applicant has replied in the form of a substitute amendment because the renumbering of the claims, as requested in the Notice, necessitated changes through the Remarks. Applicant has provided a markup copy of the substitute amendment to show the changes, as compared to the last reply.

In the Specification:

Please add a paragraph to the specification before paragraph [0001] as follows.

The present application is related to pending U.S. Application 10/807,890.

Please amend paragraph [0011] as follows:

In a third prior art, shown in FIG._1C, vertically oriented and mono-dispersed CNT is grown before gate fabrication and the gate aperture is self-aligned with a diameter of at least 2 micrometers. The spacing between CNTs has to be controlled to at least 5 micrometers so that there will be only one CNT in each gate hole. To achieve such a growth, e-beam lithography [[has to be]] was used to pattern the catalyst into an array of dots with desirable spacing and dot size, even though the fabrication of a self-aligned gate aperture does not require lithography.

Please amend paragraph [0034] as follows:

In accordance with the current invention, the gate aperture will always be perfectly aligned with the emitter, and the distance between aperture and its emitter will be substantially the same over the entire substrate surface, on the order of 100 nm, and controllable by the thickness of the gate insulator. And, all the emitters have substantially the same length and diameter. A gated field emission electron source with these characteristics [[warrantee]]provides an extra low voltage modulation, uniform emission over large area, and low energy loss from gate current. Since the emitter is largely embedded in a dielectric, it is mechanically and chemically protected and, to some extent, shielded from ion bombardment, giving rise to a longer lifetime and steadier electron emission. With a proper selection, the embedding material can also enhance the thermal conduction from the emitter. When a dielectric is used as the embedding material, the relatively large gap between the cathode and the gate electrodes also reduces the occurrence of a short circuit between them and the capacitive energy consumption during the emission modulation, resulting in a higher production yield and [[a]]higher energy efficiency. An array of emitters with a density as high as $10^8/cm^2$ will produce a more homogeneous emission compared to those of low emitter density.

Please amend paragraph [0069] as follows:

FIG. 4 shows an alternative way of fabricating the self-aligned gate aperture in accordance with the current invention. Repeating the steps described above until the deposition of the gate metal as is shown in FIG. 4A. Here the gate metal does not have to be thinner than the conformal insulator layer and it does not have to be deposited by a line-of-sight process [[n]]either. When a CMP is then applied to remove the posts 56 and stop at the gate metal on the floor surface, an aligned gate aperture around each of the CNTs automatically forms. A slight etch back of the gate insulator is then applied, forming aligned apertures in the insulator to further expose the protruding portion of the CNTs in the emitter layer for emitting electrons, as is shown in FIG. 4B.

Please amend paragraph [0072] as follows:

FIG. 6 shows a pattern of catalyst dots 50 formed from a deposition through an ion-track-etched membrane. A membrane with a pore density of $10^8/cm^2$ will result in an array of CNT with an average spacing of one micrometer between them, which is sufficiently ample for a gated structure that the diameter of the aperture is only a small fraction of it. There is a wide selection range for these track-etched membranes. Depending on applications, one could choose a membrane with a pore density anywhere between $10^5/cm^2$ and $5x10^8/cm^2$, giving rise to an average spacing between 50 micrometers to 500 nm. As for pore size, only those with pores less than 300 nm should be used since a catalyst dot size larger than 300 nm will result in multiple CNT growth. The most common track-etched membranes are those of polycarbonate or polyester. To eliminate the outgasing of these plastics in a vacuum deposition chamber, one could use a membrane from other materials such as Cu or Al thin films. Using the track etched plastic membrane as an etch mask, one can easily transfer the pores size and distribution from the plastic film to that of other materials.

In the Claims:

Please cancel without prejudice or surrender of subject matter claims 1-37. Please add the claims as indicated below. This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claims 1-37 (Canceled)

~~34.~~38. (New) An emission electron source comprising:

a cathode electrode disposed on a substrate, the cathode electrode for providing a source of electrons;

an emitter layer disposed over said cathode electrode and formed from a composition of an embedding material and one or a plurality of nano-structures embedded therein, the emitter layer having a surface, portions of the nano-structures ~~being truncated parallel to the surface and having portions~~ protruding above the surface to emit electrons;

an insulator disposed over the emitter layer, the insulator having one or a plurality of apertures, each exposing at least the ends of the nano-structures in the emitter layer; and

a gate electrode disposed over the insulator and having one or a plurality of apertures, wherein each aperture exposes a single nano-structure and is concentrically self-aligned with the end of ~~one of the nano-structures, so as to expose a single nanostructure and provide each~~the nano-structure ~~with substantially the same emitter to gate distance~~, the gate electrode being operative to control the emission of electrons through the apertures from the exposed nano-structures;

wherein the nano-structures have a coating for enhanced field emission performance.

~~35.~~39. (New) An emission electron source comprising:

a cathode electrode disposed on a substrate, the cathode electrode for providing a source of electrons;

an emitter layer disposed over said cathode electrode and formed from a composition of an embedding material and one or a plurality of nano-structures embedded therein, the emitter layer having a surface, portions of the nano-structures ~~being truncated parallel to the surface and having portions~~ protruding above the surface to emit electrons;

an insulator disposed over the emitter layer, the insulator having one or a plurality of apertures, each exposing at least the ends of the nano-structures in the emitter layer; and

a gate electrode disposed over the insulator and having one or a plurality of apertures, wherein each aperture exposes a single nano-structure and is concentrically self-aligned with the end of ~~one of the nano-structures, so as to expose a single nanostructure and provide each~~the nano-structure ~~with substantially the same emitter to gate distance~~, the gate electrode being operative to control the emission of electrons through the apertures from the exposed nano-structures.

~~36.~~40. (New) An electron source as recited in claim ~~35,~~39, wherein said nano-structures are substantially vertical.

~~37.~~41. (New) An electron source as recited in claim ~~35,~~39, wherein said nano-structures are individually spaced apart.

~~38.~~42. (New) An electron source as recited in claim ~~35,~~39, wherein said emitter-to-gate distance for each nano-structure is substantially less than one micrometer.

~~39.~~43. (New) An electron source as recited in claim ~~35,~~39, wherein the nano-structures have a surface density substantially higher than $10^6/cm^2$.

~~40.~~44. (New) An electron source as recited in claim ~~35,~~39, wherein the nano-structures protrude above the surface of the emitting layer for not more than half of one micrometer.

~~41.~~45. (New) An electron source as recited in claim ~~35,~~39, wherein the apertures in the insulator expose the entire protrusion portion of the nano-structures in the emitting layer.

~~42.~~46. (New) An electron source as recited in claim ~~35,~~39, wherein the nano-structures have at least one of their three dimensions in the nanometer range.

~~43.~~47. (New) An electron source as recited in claim ~~35,~~39, wherein the nano-structures include nano-tubes, nano-wires, nano-fibers, and nano-cones.

~~44.~~48. (New) An electron source as recited in claim ~~35,~~39, wherein the nano-structures have a coating for enhanced field emission performance.

~~45.~~49. (New) An electron source as recited in claim ~~35,~~39, wherein the nano-structures are selected from a group of materials consisting of carbon, refractory metals and alloys, conductive ceramics, conductive ceramic composites, and doped semiconductors.

~~46.~~50. (New) An electron source as recited in claim ~~45,~~49, wherein the carbon includes carbon nano-tube, carbon nano-fiber, and carbon nano-cone.

~~47.~~51. (New) An electron source as recited in claim ~~35,~~39, wherein the nano-structures comprise a nonconductive core and a conductive shell.

~~48.~~52. (New) An electron source as recited in claim ~~47,~~51, wherein the nonconductive core is made from one of wide band gap semiconductors, including diamond, BN, AlN, AlGaN, GaN, GaAs, SiC, and ZnO.

~~49.~~53. (New) An electron source as recited in claim ~~35,~~39, wherein the embedding material is comprised of at least two layers.

~~50.~~54. (New) An electron source as recited in claim ~~49,~~53, wherein the first layer of the embedding material is conductive.

~~51.~~55. (New) An electron source as recited in claim ~~35,~~39, wherein the insulator and the embedding material are composed of the same dielectric material.

~~52.~~56. (New) An electron source as recited in claim ~~35,~~39, wherein said insulator functions also as the embedding material.

~~53.~~57. (New) An electron source as recited in claim ~~35,~~39,

wherein the cathode electrode is configured as a plurality of electrically isolated cathode electrodes, each for supplying an independent source of electrons;

wherein the gate electrode is configured as a plurality of electrically isolated electrodes, each intersecting with said cathode electrodes and having one or a plurality of apertures at each intersections, each gate electrode being operative to control the emission of electrons through the apertures along the gate electrode; and

wherein activation of a selected cathode and a selected gate electrode determines an intersection where the nano-structures emit electrons.

~~54.~~58. (New) An electron source comprising:

a substrate;

electrode means, disposed over the substrate, for providing a source of electrons;

means, disposed over the source means, for emitting electrons provided by the source means, the emitting means including a one or a plurality of nano-structure emitting means for providing a flow of electrons and means for supporting the nano-structure emitting means;

an insulator disposed over the emitting means; and

one or a plurality of gating means, disposed over the insulator, for controlling the flow of electrons emitted by the nano-structure emitting means, each of said gating means arranged symmetrically relative to one of the nano-structure emitting means.

~~55.~~59. (New) An electron source as recited in claim ~~54,~~58, wherein the insulator and the gating means each include one or more apertures that expose the nano-structure emitting means.

~~56.~~ 60. (New) An electron source as recited in claim ~~54,~~58, wherein the nano-structure emitting means has at least one of its three dimensions in the nanometer range.

~~57.~~61. (New) An electron source as recited in claim ~~54,~~58, wherein the nano-structure emitting means includes carbon nano-tube, carbon nano-fiber, and carbon nano-cones.

~~58.~~62. (New) An electron source as recited in claim ~~54,~~58, wherein the nano-structure emitting means is substantially vertical.

~~59.~~63. (New) An electron source as recited in claim ~~54,~~58, wherein the nano-structure emitting means is an array of individually spaced apart nano-structures.

~~60.~~ 64. (New) A display comprising:

an electron source that includes:

a cathode electrode disposed on a substrate, the cathode electrode for providing a source of electrons;

an emitter layer disposed over said cathode electrode and formed from a composition of an embedding material and one or a plurality of nano-structures embedded therein, the emitter layer having a surface, portions of the nano-structures ~~being truncated parallel to the surface and having portions~~ protruding above the surface to emit electrons;

an insulator disposed over the emitter layer, the insulator having one or a plurality of apertures, each exposing at least the ends of the nano-structures in the emitter layer; and

a gate electrode disposed over the insulator and having one or a plurality of apertures, wherein each aperture exposes a single nano-structure and is concentrically self-aligned with the end of ~~one of the nano-structures, so as to expose a single nanostructure and provide each~~the nano-structure ~~with substantially the same emitter-to-gate distance~~, the gate electrode being operative to control the emission of electrons through the apertures from the exposed nano-structures; and

an anode plate including a transparent anode electrode disposed over a glass substrate and a phosphor screen disposed over the anode electrode, the anode plate being positioned opposite to said electron source with a vacuum gap disposed therebetween;

wherein electrons are emitted from said nano-structures by applying a voltage between said cathode and gate electrodes, and are made incident on said phosphor screen to make luminous said phosphor screen.

~~61.~~65. (New) A display as recited in claim ~~60,~~64, wherein the nano-structures are substantially vertical.

~~62.~~66. (New) A display as recited in claim ~~60,~~64, wherein the emitter-to-gate distance for each emitter is substantially less than one micrometer.

~~63.~~67. (New) A display as recited in claim ~~60,~~64, wherein the nano-structures have a surface density substantially higher than $10^6/cm^2$.

~~64.~~68. (New) A display as recited in claim ~~60,~~64,

wherein the cathode electrode is configured as a plurality of strip-like cathode electrodes extending substantially in the same direction in such a manner as to be spaced from each other at intervals in the transverse direction, each cathode strip for providing an independent source of electrons;

wherein the gate electrode is configured as a plurality of strip-like gate electrodes extending in such a manner as to intersect said plurality of cathode electrodes and to be spaced from each other at intervals in the transverse direction, and having one or a plurality of apertures at each intersection, each gate electrode for controlling the emission of electrons through the apertures along the gate electrode; and

wherein the anode electrode is configured as a plurality of strip-like anode electrodes each extending in such a manner as to be opposed to the corresponding one of said gate electrodes.

69. (New) An electron source as recited in claim 39, wherein said nano-structures in the emitter layer are truncated to substantially the same length, so that each exposed nano-structure in the gate aperture has substantially the same gate-to-emitter distance.

70. (New) An electron source as recited in claim 69, wherein said nano-structures are truncated by chemical mechanical planarization.

71. (New) An electron source as recited in claim 39, wherein said nano-structures are grown using a template and said template is at least part of the embedding material.

72. (New) An electron source as recited in claim 58, wherein said supporting means is provided by embedding portion of the nano-structure emitting means.

73. (New) An electron source as recited in claim 59, wherein said nano-structure emitting means each has substantially the same distance to the gating means.

74. (New) An electron source as recited in claim 63, wherein said nano-structures are truncated to substantially the same length.

75. (New) A display as recited in claim 64, wherein said nano-structures in the emitter layer are truncated to substantially the same length, so that each exposed nano-structure in the gate aperture has substantially the same gate-to-emitter distance.

REMARKS

Claims 1-~~33~~37 are pending in the above-referenced application. Claims 24-~~33~~37 have been withdrawn from consideration. Claims 1-10, 14-16, 18, and 20-22 are rejected. Claims 11-13, 17, 19, and 23 are objected to. The Office Action is non-final. More specifically and in accord with the item numbers therein, the Office Action has:

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In Item 2, rejected claims 1-10, 14-16, ~~18~~18, and 21-22 under 35 U.S.C. 102(e) as being anticipated by Choi (U.S. Patent No. 6,538,367); and

In Item 3, indicated that claims 11-13, 17, 19 and 23 are allowable, if rewritten in dependent form including all of the limitations of the base claim and any intervening claims.

Applicant has cancelled claims 1-~~33~~37 without prejudice or surrender of subject matter and added claims ~~34 to 64.~~38 through 75. Reconsideration is requested in light of added claims and remarks. The new independent claims are ~~34, 35, 54,~~38, 39, 58, and ~~60, the first~~64, claim 38 corresponding to allowable subject matter rewritten in independent form. Claim ~~35~~39 is an amended version of originally-submitted claim 1 and claim ~~60~~64 is an amended version of originally-submitted claim 20. Claim ~~54~~58 is new.

With respect to Item 2 and regarding claims ~~35~~38, 39, and ~~60,~~64, Applicant submits that the Choi '367 reference fails to teach each and every limitation of Applicant's invention as recited in those claims, because the reference fails to teach the limitation "a gate electrode disposed over the insulator and having one or a plurality of apertures, wherein each aperture exposes a single nano-structure and is concentrically self-aligned with the end of ~~one of the nano-structures, so as to expose a single nanostructure and provide each~~the nano-structure ~~with substantially the same emitter-to-gate distance~~, the gate electrode being operative to control the emission of electrons through the apertures from the exposed nano-structures," which is present in ~~both~~all three claims. Applicant's invention achieves this resulting structure because of the way it is fabricated. In contrast, the reference teaches the use of a particle masking technique to

achieve a gate aperture structure. However, the particle masking techniques taught in the reference cannot achieve the limitation set forth and therefore the reference does not teach such a structure. First, the technique in the reference purposefully includes a multiplicity of nanoconductors in each aperture. Choi, Col. 7, line 64 to Col. 8, line 3. In contrast, Applicant's invention, in claims ~~35~~38, 39, and ~~60~~,64, recites that each ~~of the apertures~~aperture exposes a single nano-structure and is concentrically self-aligned with ~~a protruding portion so as to expose~~ the end ~~thereof~~of the nano-structure. Second, the technique in the reference does not contemplate the alignment of an aperture about ~~each one of~~ the end of a nano-~~structures~~structure. This is clear from FIG. 11 of the reference and the description of the particle mask technique. Clearly, the range in the size of the particles (1-5 μm) is such that multiple nano-structures will become exposed by the aperture and thus there is no concept of aligning the aperture with those multiple structures. Choi, Col. 8, lines 46-53. Therefore, the Choi reference fails to teach each and every limitation of Applicant's invention as recited in claims ~~35~~38, 39, and ~~60~~.64.

With respect to claim ~~54~~,58, Applicant further submits that the Choi reference fails to teach the limitation "one or a plurality of gating means, disposed over the insulator, for controlling the flow of electrons emitted by the nano-structure emitting means, each of ~~the plurality of~~said gating means arranged symmetrically relative to one of the ~~plurality of~~ nano-structure emitting means." In the reference, there is no possibility that the structures achievable therein could have each gating means arranged symmetrically with respect to one of the nano-structures, as the reference only contemplates a plurality of nano-structures in each aperture. Choi, Col. 7, line 64 to Col. 8, line 3. Therefore, the reference fails to teach each and every limitation of claim ~~54~~.58.

With respect to claims ~~36~~40-~~53~~,57, Applicant submits that these claims are allowable at least because claim ~~35~~,39, from which they depend, directly or indirectly, is allowable. Additionally, Applicant submits that the Choi reference fails to teach the limitation "wherein the nano-structures protrude above the surface of the emitting layer for not more than half of one micrometer," in claim ~~40~~44 or the limitation "wherein the apertures in the insulator expose the entire protrusion portion of the nano-structures in the emitting layer," in claim ~~41~~,45, as nothing in Choi teaches or describes any such ~~a~~ protrusion. Additionally, Choi fails to teach or describe

the limitation "wherein the nano-structures have a coating for enhanced field emission performance," recited in claim ~~44~~48. Additionally, Choi fails to teach the limitation "wherein the nano-structures comprise a nonconductive core and a conductive shell," as recited in claim ~~47~~51 or the limitation "wherein the nonconductive core is made from one of wide band gap semiconductors, including diamond, BN, AlN, AlGaN, GaN, GaAs, SiC, ZnO," recited in claim ~~48~~52. In fact, the Examiner has indicated that the limitations of claim ~~44~~48 would make the claims allowable if rewritten in independent form. This Applicant has done in claim ~~34~~38.

Additionally, the Choi reference fails to teach the limitation "wherein the embedding material is comprised of at least two layers," recited in claim ~~49~~53, or the limitation "wherein the first layer of the embedding material is conductive," recited in claim ~~50~~54, as Choi fails to describe any features of any embedding material. Additionally, Choi fails to teach the limitation "wherein the insulator and the embedding material are composed of the same dielectric material," in claim ~~51~~55 or the limitation "wherein said insulator functions also as the embedding material," in claim ~~52~~56, again because Choi fails to describe any features of any embedding material. Additionally, Applicant submits that claim ~~53~~57 is allowable because the Choi reference fails to teach the limitation "wherein the gate electrode is configured as a plurality of electrically isolated electrodes, each intersecting with said cathode electrodes," because Choi does not describe the arrangement of intersecting electrodes. In fact, the Examiner has indicated that ~~the limitation of~~ claims ~~51~~55 and ~~53~~57 would be allowable if rewritten in independent form.

With respect to claims ~~55~~59-~~59~~63, Applicant submits that these claims are allowable at least because claim ~~54~~58, from which they depend, is allowable.

With respect to claims ~~61~~65-~~64~~68, Applicant submits that these claims are allowable at least because claim ~~60~~64, from which they depend, is allowable. Additionally, Applicant submits that the Choi reference fails to teach the limitation "wherein the cathode electrode is configured as a plurality of strip-like cathode electrodes...wherein the gate electrode is configured as a plurality of strip-like gate electrodes extending in such a manner as to intersect said plurality of cathode electrodes," recited in claim ~~64~~68, because Choi describes no such

arrangement of intersecting cathodes and gates. In fact, the Examiner has indicated that the limitation of claim ~~64,~~68, would be allowable if rewritten in independent form.

With respect to ~~claims 34,~~claim 38, as mentioned above, Applicant has rewritten originally submitted claim 11 in independent form. Applicant therefore believes these claims are allowable.

Thus, in light of the above, Applicants respectfully request reconsideration and allowance of the pending claims and the new claims in the above-mentioned application.

Respectfully submitted,

Dated: December 1, 2005

Anthony B. Diepenbrock III
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CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that this correspondence is being forwarded via facsimile to Examiner Jessy Fenty in Group No. 2815 at facsimile number 571.273.8300 located at Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA, 22313-1450, on

Date: December 1, 2005

Yolette Yturralde-Owen